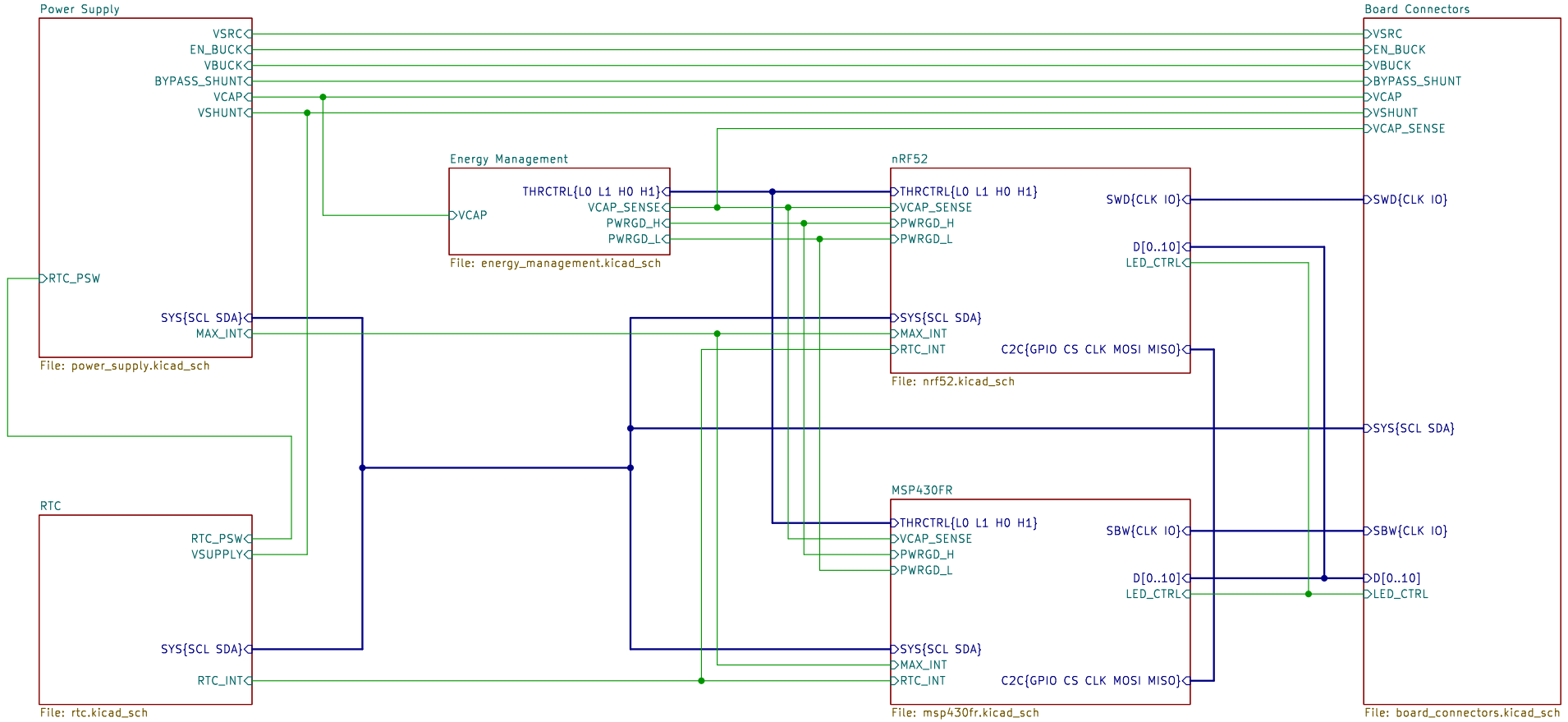
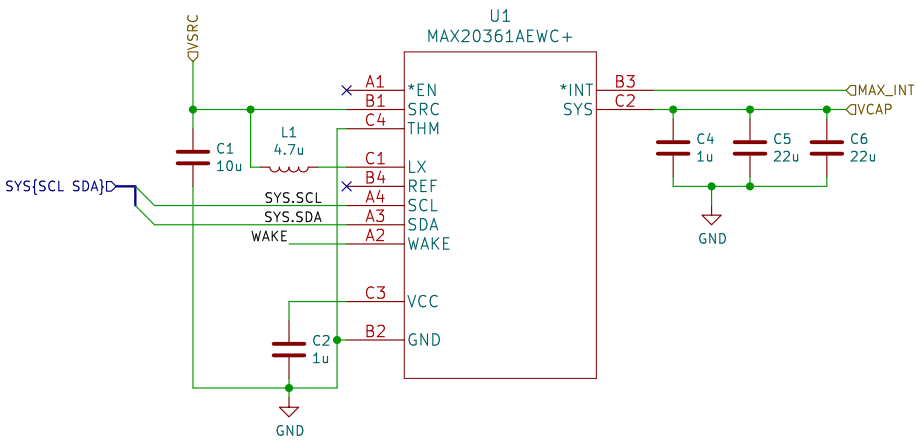


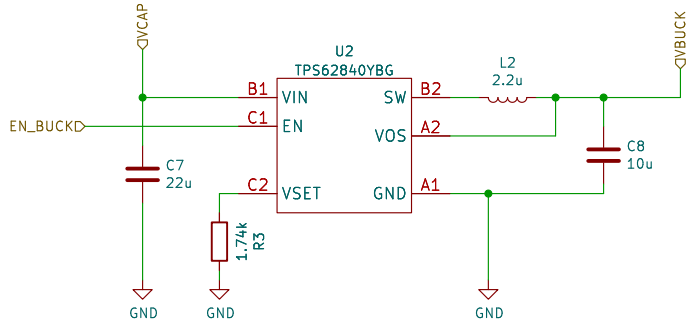
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File: voltix-module.kicad_sch

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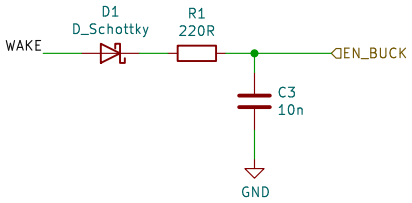
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.3		Id: 1/7



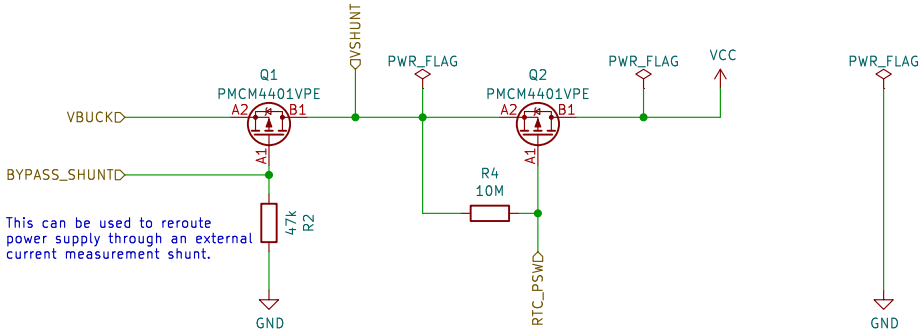
DC–DC boost with MPPT to step up voltage from harvester at VSRC. Configured via I2C. Charges capacitor on VCAP.



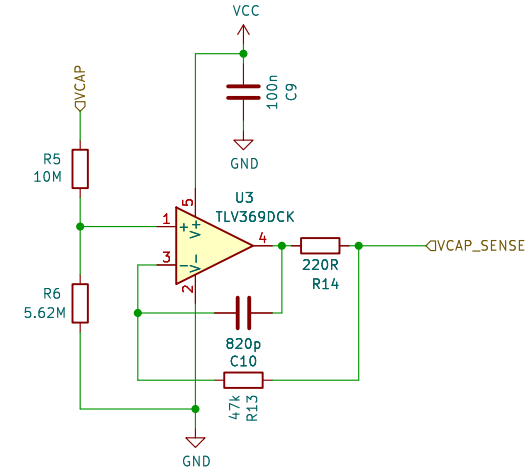
DC–DC buck regulates capacitor voltage to 2.0V. Gets activated by WAKE signal from MAX20361.



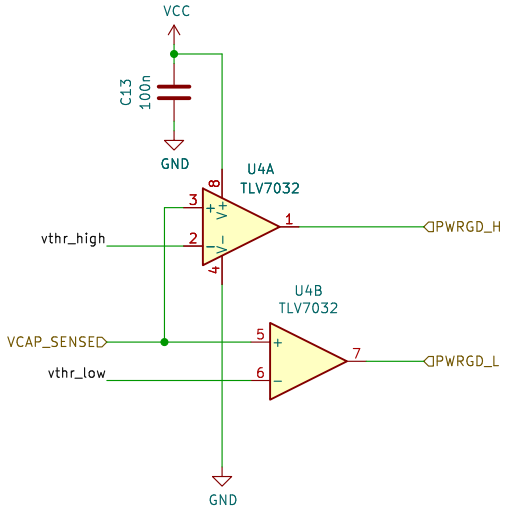
After switching on, capacitor voltage drops and 'wake' signal from MAX20361 goes low again.
This circuit keeps the buck on for long enough to disable the 'wake' functionality.



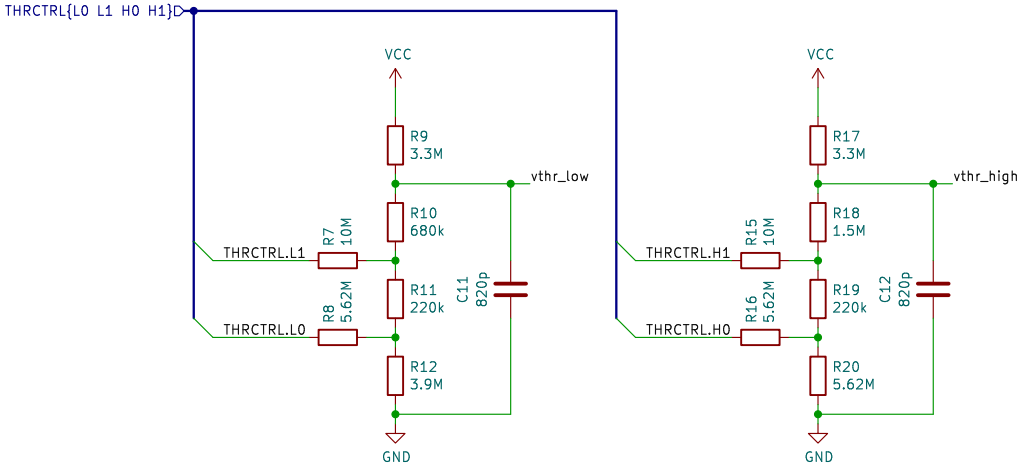
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Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.3		Id: 2/7



Voltage divider and op-amp buffer for capacitor voltage.
Range: 0V..4.8V->0V..1.727V.



Power OK comparator with hysteresis. Signals to nRF if capacitor is within vthr_on and vthr_off.

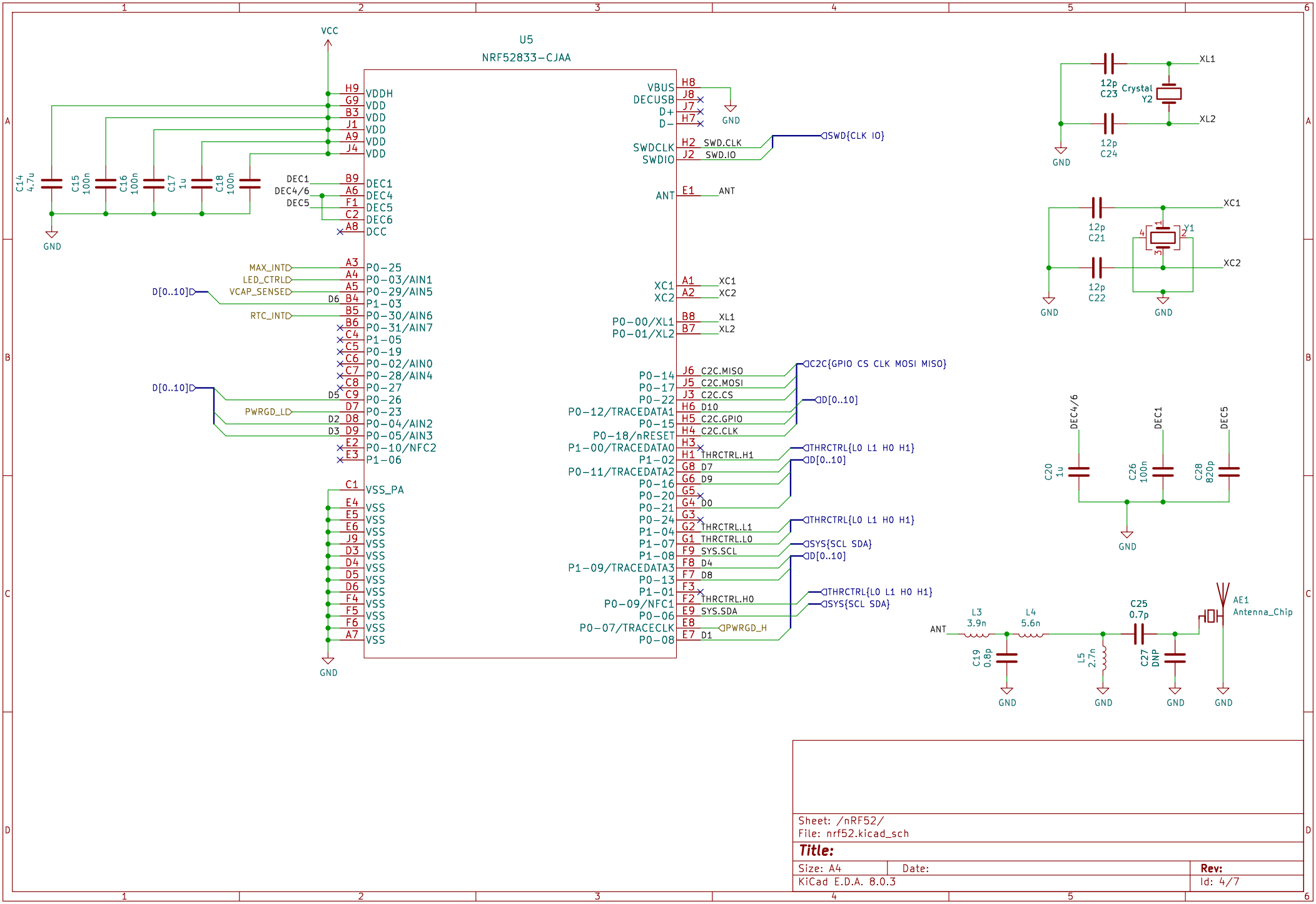


Resistor networks use tri-state gpios to provide 9 comparator threshold levels.

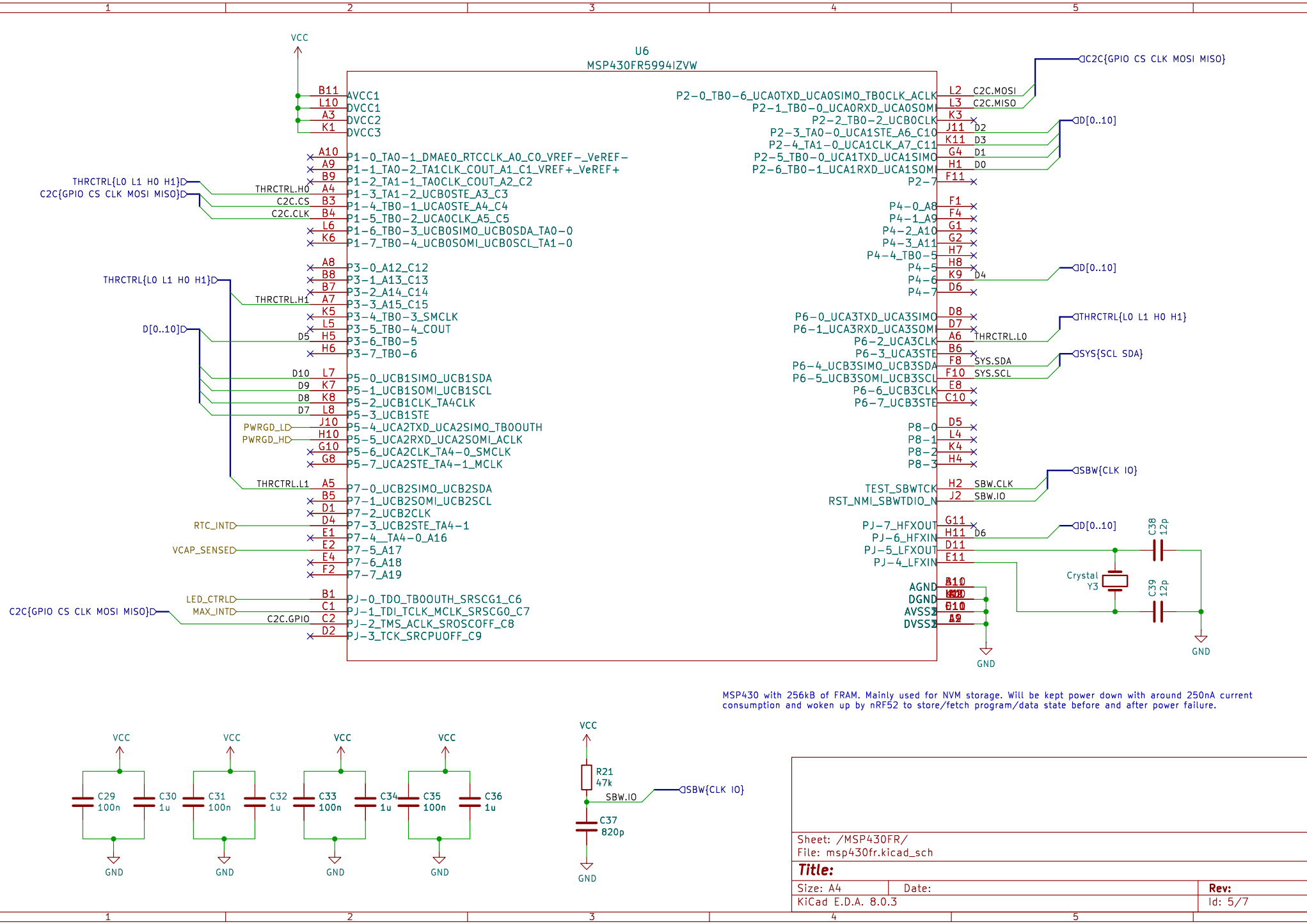
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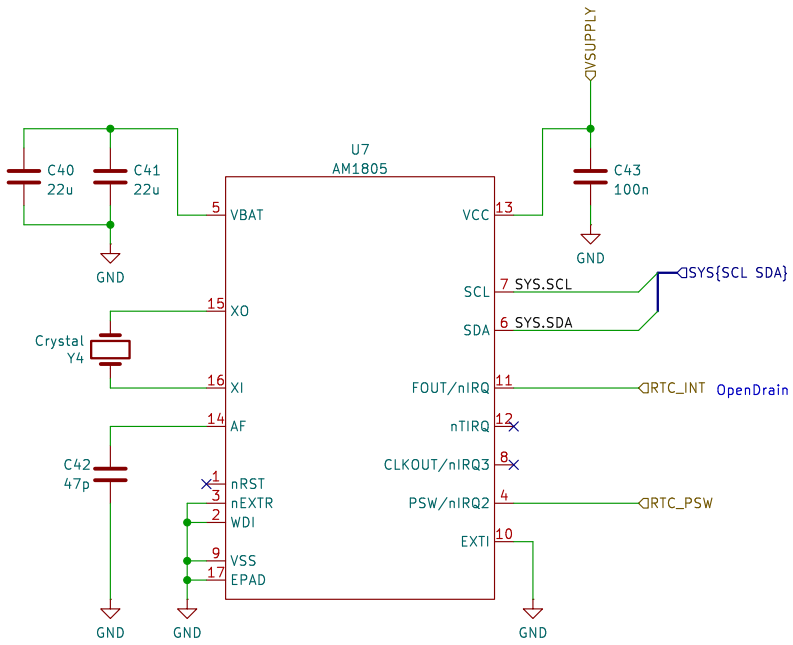
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KiCad E.D.A. 8.0.3		Id: 3/7

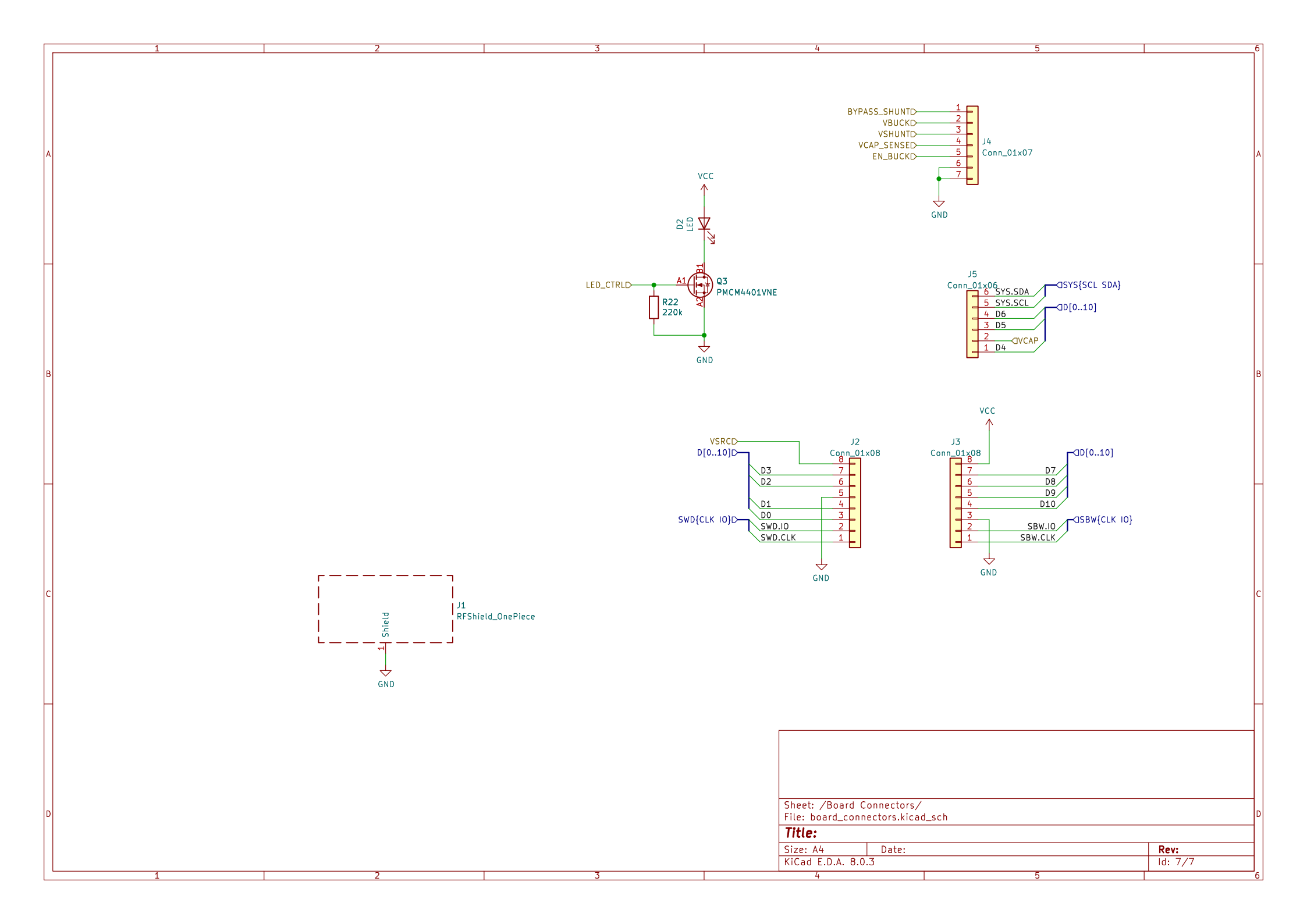


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Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.3		Id: 4/7


U6
MSP430FR5994IZVW
VCC
B11 AVCC1
L10 DVCC1
A3 DVCC2
K1 DVCC3
A10 P1_0_TA0_1_DMAE0_RTCCLK_A0_C0_VREF−_VeREF−
A9 P1_1_TA0_2_TA1CLK_COUT_A1_C1_VREF+_VeREF+
B9 P1_2_TA1_1_TA0CLK_COUT_A2_C2
THRCTRL{L0 L1 H0 H1}
THRCTRL.H0 A4 P1_3_TA1_2_UCB0STE_A3_C3
C2C{GPIO CS CLK MOSI MISO}
C2C.CS B3 P1_4_TB0_1_UCA0STE_A4_C4
C2C.CLK B4 P1_5_TB0_2_UCA0CLK_A5_C5
L6 P1_6_TB0_3_UCB0SIMO_UCB0SDA_TA0_0
K6 P1_7_TB0_4_UCB0SOMI_UCB0SCL_TA1_0
A8 P3_0_A12_C12
B8 P3_1_A13_C13
THRCTRL{L0 L1 H0 H1}
B7 P3_2_A14_C14
THRCTRL.H1 A7 P3_3_A15_C15
K5 P3_4_TB0_3_SMCLK
D[0..10]
L5 P3_5_TB0_4_COUT
D5 H5 P3_6_TB0_5
H6 P3_7_TB0_6
D10 L7 P5_0_UCB1SIMO_UCB1SDA
D9 K7 P5_1_UCB1SOMI_UCB1SCL
D8 K8 P5_2_UCB1CLK_TA4CLK
D7 L8 P5_3_UCB1STE
PWRGD_L J10 P5_4_UCA2TXD_UCA2SIMO_TB0OUTH
PWRGD_H H10 P5_5_UCA2RXD_UCA2SOMI_ACLK
G10 P5_6_UCA2CLK_TA4_0_SMCLK
G8 P5_7_UCA2STE_TA4_1_MCLK
THRCTRL.L1 A5 P7_0_UCB2SIMO_UCB2SDA
B5 P7_1_UCB2SOMI_UCB2SCL
D1 P7_2_UCB2CLK
RTC_INT D4 P7_3_UCB2STE_TA4_1
E1 P7_4__TA4_0_A16
VCAP_SENSED E2 P7_5_A17
E4 P7_6_A18
F2 P7_7_A19
LED_CTRL B1 PJ_0_TDO_TB0OUTH_SRSCG1_C6
MAX_INT C1 PJ_1_TDI_TCLK_MCLK_SRSCG0_C7
C2C{GPIO CS CLK MOSI MISO}
C2C.GPIO C2 PJ_2_TMS_ACLK_SROSCOFF_C8
D2 PJ_3_TCK_SRCPUOFF_C9
P2_0_TB0_6_UCA0TXD_UCA0SIMO_TB0CLK_ACLK L2 C2C.MOSI
P2_1_TB0_0_UCA0RXD_UCA0SOMI L3 C2C.MISO
P2_2_TB0_2_UCB0CLK K3
P2_3_TA0_0_UCA1STE_A6_C10 J11 D2
P2_4_TA1_0_UCA1CLK_A7_C11 K11 D3
P2_5_TB0_0_UCA1TXD_UCA1SIMO G4 D1
P2_6_TB0_1_UCA1RXD_UCA1SOMI H1 D0
P2_7 F11
P4_0_A8 F1
P4_1_A9 F4
P4_2_A10 G1
P4_3_A11 G2
P4_4_TB0_5 H7
P4_5 H8
P4_6 K9 D4
P4_7 D6
P6_0_UCA3TXD_UCA3SIMO D8
P6_1_UCA3RXD_UCA3SOMI D7
P6_2_UCA3CLK A6 THRCTRL.L0
P6_3_UCA3STE B6
P6_4_UCB3SIMO_UCB3SDA F8 SYS.SDA
P6_5_UCB3SOMI_UCB3SCL F10 SYS.SCL
P6_6_UCB3CLK E8
P6_7_UCB3STE C10
P8_0 D5
P8_1 L4
P8_2 K4
P8_3 H4
TEST_SBWTCK H2 SBW.CLK
RST_NMI_SBWTDIO_N J2 SBW.IO
PJ_7_HFXOUT G11
PJ_6_HFXIN H11 D6
PJ_5_LFXOUT D11
PJ_4_LFXIN E11
AGND
DGND
AVSS2
DVSS2
C2C{GPIO CS CLK MOSI MISO}
D[0..10]
THRCTRL{L0 L1 H0 H1}
SYS{SCL SDA}
SBW{CLK IO}
C38 12p
C39 12p
Crystal
Y3
GND
MSP430 with 256kB of FRAM. Mainly used for NVM storage. Will be kept power down with around 250nA current consumption and woken up by nRF52 to store/fetch program/data state before and after power failure.
C29 100n
C30 1u
C31 100n
C32 1u
C33 100n
C34 1u
C35 100n
C36 1u
R21 47k
SBW.IO
C37 820p
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Rev:
KiCad E.D.A. 8.0.3
Id: 5/7



Sheet: /RTC/		
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KiCad E.D.A. 8.0.3		Id: 6/7



Sheet: /Board Connectors/
File: board_connectors.kicad_sch

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